A Variable Gain Amplifier for Wideband DCRs using 0.13µm CMOS Technology

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Abstract – A wideband variable gain amplifier (VGA) design is introduced with two different schemes. It is based on a fully differential amplifier with resistive loads, and a Negative Miller Capacitance technique is used to increase the bandwidth of the amplifier. The amplifier consists of three stages, and the gain is varied through the second and third stages, where they are degenerated by a voltage controlled variable resistance. The design is ready to be implemented with MOSFETs using UMC 0.13µm technology. The supply voltage is 1.2V, and achieved gain is up to 35 dB with a minimum bandwidth of 1 GHz. Two design schemes are discussed, describing the tradeoff between the dynamic range of the variable gain and the bandwidth.

Index Terms – Variable gain amplifier (VGA), negative miller capacitance.

I. INTRODUCTION

Wideband communications are being used in most of the wireless communication techniques, requiring a high bitrates digital modulation schemes, and multiple access techniques, as well as a multiple antennas at the receiver so as to maximize the received signal to noise ratio. This by turn requires very high speed, low power, low distortion, small area, and a low noise figure variable gain amplifier at the receiver, that’s why an MOSFET is used in the design of most microelectronic circuits.

Different design techniques of variable gain amplifier (VGA) are discussed in many publications. Some designs are of a very low bandwidth [1]-[3], which is not suitable for wideband receivers; other designs used non – linear functions to control the voltage gain, such as an exponential controller [4]. Many articles cover the design methodology of wideband variable gain amplifier (VGA), where inductors are used to increase the bandwidth using the inductive peaking technique without affecting the stability of the amplifier [5], but the use of inductors requires a large chip area, which is inconvenient for many of the wideband mobile receivers. One of the most used techniques to achieve wideband requirements without using inductors is introduced in [6]-[8]. This is known as “Cherry – Hooper” amplifier, where a negative feedback is used to decrease the effect of the capacitive loading and thus increasing the bandwidth, but the main disadvantage of this technique is the limitation of the output voltage headroom due to the decreased output swing, and this will lead to more power consumption and can’t be used for low power applications.

In this paper, a wideband variable gain amplifier (VGA) is described. It comprises three stages based on a fully differential amplifier with resistive loads instead of active loads, so it will not affect the output swing keeping the output voltage headroom maximum. The negative Miller capacitance technique is used to increase the bandwidth. Two implementations of the (VGA) are discussed showing that there exists a tradeoff between the dynamic range and the bandwidth.

The paper is organized as follows, the architecture of the (VGA) is described in section II. The analysis of the circuit and the design parameters are held in section III. Simulation results are shown and explained in section IV. Finally, the conclusion and proposals for future work are summarized in section V.

II. VARIABLE GAIN AMPLIFIER (VGA) ARCHITECTURE

The (VGA) described through this paper consists of three stages; a low noise input stage with constant gain, and two variable gain stages. The number of stages is chosen to achieve a high gain – bandwidth product, while keeping the noise figure of the (VGA) minimum. The optimum value was determined using MATLAB simulations.

The schematic of the first stage of the amplifier is shown in Fig. 1. The input of the amplifier is two NMOS transistors forming a differential pair, which is resistively loaded. The amplifier is driven by a tail current source, which is an NMOS transistor also operating in the saturation region. A common mode feedback (CMFB) amplifier is used to bias the NMOS current source with an accurate common mode voltage, so as to minimize the effect of
mismatch between the two branches of the amplifier. The (CMFB) senses the output common mode voltage and compares it with a reference voltage, and thus any change in the output common mode level would be compensated by the (CMFB). The (CMFB) is a simple differential pair with an active load current mirror, and the capacitor ($C_f$) connecting the output of the (CMFB) to the drain of the tail MOSFET current sources is added to enhance the phase margin and hence the stability of the (VGA). The use of the (CMFB) results in a differential voltage gain of almost 1 dB less than that without using (CMFB). Two capacitors provide feedback from the output of one of the two input NMOS transistors to the input of the other and vice versa. This technique is known as the negative Miller capacitance and is widely used to obtain a high bandwidth inductorless amplifier [5,9]. The values of these capacitors must be chosen to be equal to the equivalent input capacitances of the subsequent amplifier, so that they cancel the effect of the pole resulting from these parasitic capacitances.

The schematic of stages two and three are shown in Fig. 2. They are merely the same as stage one but with the input NMOS transistors degenerated by a variable resistance used to control the gain. This voltage controlled variable resistance is implemented using a cascade of NMOS transistors operating in the triode region, and changing the voltage applied to their gates changes their resistances. There’s a drawback in this variable resistance implementation in that it will result in a non-linear resistance. Some publications introduced different ways to implement a more linear resistance using only MOSFETs. A capacitor is connected in parallel with the variable resistance creating a zero in the transfer function of the amplifier, and the value of this capacitor must be chosen properly so as to adjust the value of this zero to be exactly the same as the value of the dominant pole, cancelling the effect of this pole, and thus increasing the -3 dB bandwidth.

![Fig. 1](image1.png)  
**Fig. 1** Schematic of the first stage of the (VGA).

![Fig. 2](image2.png)  
**Fig. 2** Schematic of the second and third stages of the (VGA).

III. VGA ANALYSIS AND DESIGN

The design of the (VGA) is carried out by designing each of the three stages separately, so that the design goals of the (VGA) are achieved. Since the gain – bandwidth product of the (VGA) is constant, the bandwidth of each stage can be calculated from the total bandwidth as follows [11]

\[
BW = BW_{\text{total}} \cdot \left(2^{1/n} - 1 \right)^{\frac{3}{2}},
\]

where $n$ is the number of identical stages. The bandwidth of each stage is calculated from (1) and was found to be greater than 2 GHz to achieve a minimum total bandwidth of 1 GHz.

From the small signal analysis of the first stage amplifier, the voltage gain can be written as

\[
A_{v1}(s) = \frac{A_{\text{vol}}}{1 + \frac{s}{P_{1,1}}} \cdot \frac{1 + \frac{s}{P_{2,1}}}{1 + \frac{s}{P_{3,1}}},
\]

where $A_{\text{vol}}$ is the large signal voltage gain, $P_{1,1}$ and $P_{2,1}$ are the poles of the amplifier, and are given as

\[
A_{\text{vol}} = g_m \cdot R_{D1},
\]
\[ P_{1j} = \left( R_{Dj} \cdot C_{Lj} \right)^{-1}, \quad (4) \]
\[ P_{2j} = \left( R_{Gj} \cdot C_{Gj} \right)^{-1}, \quad (5) \]

where \( g_m \) is the transconductance of the input NMOS transistors, \( R_{Dj} \) is the load resistance, \( C_{Lj} \) is the equivalent load capacitance seen at the output of the amplifier, \( R_{Gj} \) is the resistance of the input source, and \( C_{Gj} \) is the input parasitic capacitance seen between the gate and source of the input NMOS transistors. The value of \( (R_{Dj}, C_{Lj}) \) is much greater than the value of \( (R_{Gj}, C_{Gj}) \), which makes \( (P_{1j}) \) the dominant pole. The effect of the load resistance on the gain of the amplifier is stronger than that of the input transistors, which means that for larger gain values \( (R_{Dj}) \) has to be increased, but this will affect the dominant pole decreasing it, and thus decreasing the bandwidth.

Applying the small signal analysis to stages two and three as well will yield

\[
A_{s2}(s) = A_{v2} \cdot \frac{1 + \frac{s}{Z_{1,2}}}{\left[ 1 + \frac{s}{P_{1,2}} \right] \left[ 1 + \frac{s}{P_{2,2}} \right] \left[ 1 + \frac{s}{P_{3,2}} \right]}, \quad (6)
\]

where \( A_{v2} \) is the large signal gain of stages two and three, \( Z_{1,2} \) is the zero resulting from the variable resistance and the capacitor parallel to it, and \( P_{1,2}, P_{2,2}, \text{ and } P_{3,2} \) are the poles and are given as

\[
A_{v2} = g_m2 \cdot R_{D2}, \quad (7)
\]
\[
Z_{1,2} = \left( R_s \cdot C_s \right)^{-1}, \quad (8)
\]
\[
P_{1,2} = \frac{1 + \left( g_m2 \cdot R_s / 2 \right)}{R_{g2} \cdot C_{g2} + R_s \left( C_s + \left( C_{g2} / 2 \right) \right)}, \quad (9)
\]
\[
P_{2,2} = \left( R_s \cdot C_s \right)^{-1} + \left( R_{g2} \cdot C_{g2} \right)^{-1} + \left( 2 \cdot R_{g2} \cdot C_s \right)^{-1}, \quad (10)
\]
\[
P_{3,2} = \left( R_{D2} \cdot C_{L2} \right)^{-1}, \quad (11)
\]

where \( g_m2 \) is the transconductance of the input NMOS transistors of stages two and three, \( R_{D2} \) is the load resistance, \( R_s \) is the voltage controlled variable resistance responsible for varying the gain of the amplifier, \( C_s \) is the capacitor connected parallel to \( R_s \), \( R_{g2} \) is the resistance of the driving source at the input of the amplifier, \( C_{g2} \) is the amplifier’s equivalent parasitic input capacitance. By increasing the voltage at the gates of the NMOS transistors forming \( R_s \), its resistance decreases and thus increasing the gain of the amplifier. The value of \( C_s \) must be chosen to assure that the zero of the amplifier and the dominant pole coincide and cancel each other, thus increasing the bandwidth of the amplifier. Unfortunately it is hard to control the capacitance value so that it increases by exactly the same amount that \( R_s \) has decreased, which will result in an undesired peaking in the frequency response of the amplifier. Assuming that the value of the zero is adjusted to perfectly match that of the dominant pole and cancel each other, the expression of the voltage gain can be written as

\[
A_{v2}(s) = -\frac{g_m2 \cdot R_{D2}}{1 + g_m2 \cdot R_s / 2} \cdot \frac{1 + \frac{s}{P_{2,2}}}{\left( 1 + \frac{s}{P_{2,2}} \right) \left( 1 + \frac{s}{P_{3,2}} \right)}, \quad (12)
\]

so \( P_{2,2} \) will appear as if it is the dominant pole which is much larger than \( P_{1,2} \), resulting in a larger bandwidth.

**IV. SIMULATION RESULTS**

Simulations are made to show the total range of the variable gain of the amplifier, and the frequency response for different control voltages. In Fig. 3, sweeping the control voltage shows that the amplifier can achieve a variable gain range about 15 dB with a minimum bandwidth of about 1.8 GHz. The control voltage is varied from 0.67 V to 0.9 V resulting in a variable gain from 20 dB to 34 dB, as shown in Fig. 4. Some modifications are made to increase the range of the variation of the gain, but this results in decreasing the bandwidth of the amplifier. Fig. 5 shows the simulations of the amplifier after the modifications, and the results shows that the gain range increased to reach 20 dB.
with a minimum bandwidth of 1 GHz. The frequency response is given in Fig. 6 for the same control voltage, showing that the gain is varied from 12 to 35 dB. The peaking in the frequency response for low control voltages is due to the imperfect matching of the values of the zero and the dominant pole of the amplifier, which resulted from the value of $C_s$. The input 1 dB compression point of the (VGA) is given in Fig. 7, which shows that the (VGA) has an input referred 1 dB compression of -18.63 dB. The third order input referred intercept point of the (VGA) is given in Fig. 8, and it shows that the (VGA) has an IIP3 of approximately -47 dB. The noise figure of the (VGA) is found to be 13 dB with an input referred noise of $3.9 \text{nV}/\sqrt{\text{Hz}}$, and the total harmonic distortion is 0.03 %. The simulated (VGA) power consumption is about 0.32 mW.

![Dynamic Range](image1.png)

**Fig. 3** The allowable variable gain range of the (VGA).

![Frequency Response](image2.png)

**Fig. 4** The frequency response of the (VGA) for various control voltages.
V. CONCLUSION AND FUTURE WORK

The design of a wideband inductorless variable gain amplifier is presented in this paper; with a negative Miller capacitance to increase its bandwidth, and can be operated using a supply voltage of 1.2 V. The design and simulations are carried out using 0.13μm technology. The amplifier can be designed using 0.09μm technology to increase the bandwidth of the amplifier.

![Dynamic Range](image1)

Fig. 5 The allowable variable gain range of the (VGA) after modification.

![Frequency Response](image2)

Fig. 6 The frequency response of the (VGA) for various control voltages after modification.

REFERENCES


Fig. 7 Input 1 dB compression point of the (VGA).

Fig. 8 Third order input referred intercept point (IIP3) of the (VGA).